2.5 Gbit/s CMOS transimpedance amplifier for optical communication applications

Sung Min Park and Hoi-Jun Yoo

A 2.5 Gbit/s transimpedance amplifier is realised using a 0.6 μm CMOS technology. By exploiting a regulated cascode configuration as the input stage, the amplifier achieves significant bandwidth improvement. The measured results demonstrate 2.2 GHz bandwidth for 0.5 pF photodiode capacitance with 55.3 dBΩ transimpedance gain.

Introduction: Low-cost CMOS technologies are very attractive for the integration of mixed-mode circuits in a single chip, thereby providing a good solution for optical communication applications. However, the main bottleneck of CMOS technologies is its inherent lower speed and larger parasitic capacitance than others such as GaAs, InP-based materials, or HEMTs. In particular, the high-speed front-end circuits of optical receivers are difficult to realise with CMOS processes since they are exposed to a number of trade-offs between high speed, high gain, low noise and low power consumption. Hence, much research has been conducted for gigabit optical front-end circuits [1–4]. Even though the latest report demonstrated a 10 Gbit/s front-end transimpedance amplifier (TIA) [1], it was realised in a still costly 0.18 μm CMOS technology. Previously, a 2.5 Gbit/s common-drain-type TIA with a 0.35 μm CMOS technology was reported using inductive peaking technique [2]. However, no measured eye diagrams were given and the bandwidth (1.45 GHz) was insufficient to achieve 2.5 Gbit/s operation for a NRZ signal. In this Letter, a 2.5 Gbit/s single-ended TIA is implemented in a 0.6 μm CMOS technology, which exploits a regulated cascode (RGC) circuit to achieve significant bandwidth improvement despite poor device characteristics [3].

Circuit description: Fig. 1 shows the schematic diagram of the RGC TIA. The regulated cascode input provides the virtual-ground input resistance of $1/g_{m1}(1+g_{mB}R_B)$, where $(1+g_{mB}R_B)$ is the voltage gain of the local feedback stage (M_B and R_B) [3, 4]. Thus, it efficiently isolates the large input parasitic capacitance (including the photodiode capacitance C_{pd}) from the bandwidth determination, resulting in a potential for wide-bandwidth. The dominant pole of the amplifier is determined by the time constant (τ_1) at the highest impedance node which is the drain of M_1:

$$\tau_1 = (R_1 \parallel R_f)\,(C_{d1} + C_{g2} + C_f) = \frac{1}{p_1} \tag{1}$$

where C_{d1} is the total drain capacitance of M_1, C_{g2} is the total gate capacitance of M_2, R_f is the feedback resistance, and C_f is the parasitic capacitance of R_f.

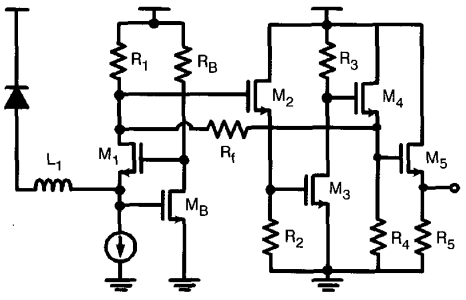

Fig. 1 *Schematic diagram of RGC transimpedance amplifier*

The non-dominant pole is determined by the time constant (τ_2) at the gate of M_3:

$$\tau_2 = \left(\frac{1}{g_{m2}} \parallel R_2\right)[C_{s2} + C_{gs3} + (1+g_{m3}R_3)C_{gd3}] = \frac{1}{p_2} \tag{2}$$

where C_{s2} is the total source capacitance of M_2, C_{g3} is the total gate capacitance of M_3, and $g_{m3}R_3$ is the voltage gain of M_3 stage.

Another pole is determined at the input node of the amplifier, but the virtual-ground input renders the input pole at higher frequency than other poles. Hence, the −3 dB bandwidth of the RGC TIA is approximately given by,

$$f_{-3dB} \cong \frac{(2+g_{m3}R_3)}{2\pi R_f[C_{d1} + C_{g2} + (1+g_{m3}R_3)C_f]} \tag{3}$$

It is noted that the bandwidth increases with the voltage gain of $g_{m3}R_3$. Since the voltage gain cannot be increased indefinitely without stability problems, it is appropriately chosen to achieve 2 GHz bandwidth with good stability.

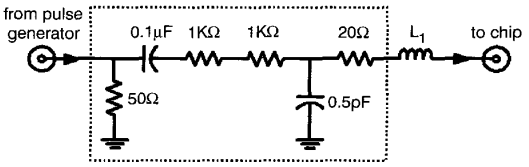

Fig. 2 *Equivalent circuit of photodiode*

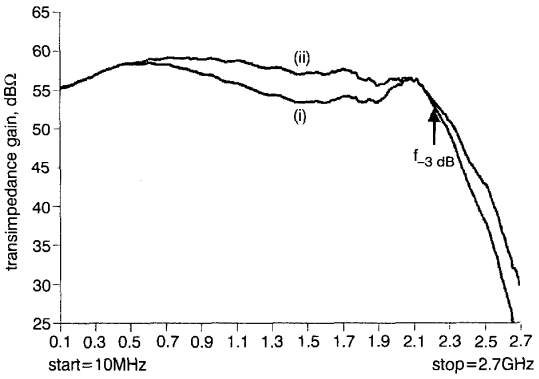

Fig. 3 *Measured frequency response of RGC TIA for C_{pd} of 0.5 pF with R_{pd} of 20 and 5 Ω*

(i) 20 Ω
(ii)5 Ω

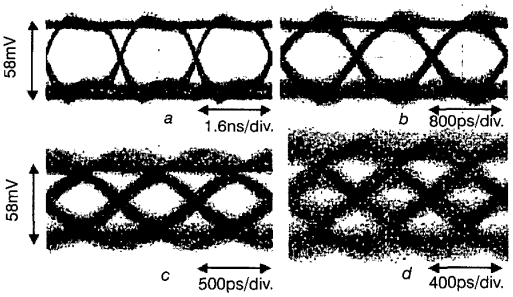

Fig. 4 *Measured eye diagrams for 100 μA $2^{31}-1$ PRBS at different bit rates (V_{out} = 58 mV)*

a 622 Mbit/s
b 1.25 Gbit/s
c 2 Gbit/s
d 2.5 Gbit/s

Measured results: Test chips were fabricated using a digital 0.6 μm CMOS process. For facilitating the measurements, the photodiode is modelled as a current source with 0.5 pF parasitic capacitance and 20 Ω parasitic resistance (shown in Fig. 2) and mounted with a test-chip on an FR-4 PC-board. Frequency response is measured in the range of 10 MHz to 2.7 GHz using a HP8753ES network analyser with a test power of −15 dBm. Fig. 3 shows that the transimpedance gain of 55.3 dBΩ is measured with the −3 dB bandwidth of 2.2 GHz for 0.5 pF photodiode capacitance. It can be seen that the gain reduction at the mid-band is attributed to the parasitic resistance (R_{pd}) of the photodiode. Fig. 4 shows the measured eye diagrams

for $2^{31}-1$ PRBS with 100 μA equivalent photocurrent at different bit rates of 622 Mbit/s, 1.25, 2 and 2.5 Gbit/s. Overshoot in the eye diagrams occurs due to the gain fluctuation in the frequency response and also to the group-delay variations. The eye diagram at 2.5 Gbit/s is not widely open which may be attributed to the peaking around 2.1 GHz. For 2 Gbit/s 2^7-1 PRBS, the sensitivity of the TIA is estimated to be −17 dBm for the bit error rate (BER) of 10^{-10}. The whole module consumes 210 mW power from a single 5 V supply.

Conclusion: A 2.5 Gbit/s regulated cascode TIA has been realised with a low-cost 0.6 μm CMOS technology. RGC input configuration efficiently isolates the large input parasitic capacitance from the bandwidth determination, resulting in 2.2 GHz bandwidth for 0.5 pF photodiode capacitance. This renders the RGC TIA suitable for OC-48 optical communication applications.

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Different index contrast silica-on-silicon waveguides by PECVD

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Ge-doped silica-on-silicon waveguides with index steps of 0.01 and 0.02 were fabricated by a combination of plasma enhanced chemical vapour deposition (PECVD) and reactive ion etching (RIE) techniques, and their characteristics, including propagation loss, coupling loss with standard singlemode fibres, minimal bend radius, and birefringence, were investigated. The waveguides have good propagation properties and small birefringence, compared to using flame hydrolysis deposition (FHD).

Introduction: Planar waveguide components play key roles in telecommunication. Among different waveguide materials germanium (Ge)-doped glass has stable performance and low propagation loss, and has become the most advanced and mature technique available [1–3]. Plasma enhanced chemical vapour deposition (PECVD) and flame hydrolysis deposition (FHD) are the two main methods used to deposit Ge-doped glass. FHD has been perfected to make silica-on-silicon waveguides, and resulted in commercialisation of various components such as splitters, wavelength division multiplexers. The first generation of Ge-doped silica-on-silicon waveguide components implements low index contrasts (<1%) in order to match the mode of standard singlemode fibres [4]. At present more and more research is concentrated on high index contrasts to construct highly-integrated and large-scale optical circuits [5].

In this Letter, Ge-doped silica-on-silicon waveguides with different index contrasts were fabricated by a combination of PECVD with reactive ion etching (RIE) techniques. The characteristics measured included propagation loss, minimal bend radius, birefringence, and coupling loss with standard singlemode. The waveguides fabricated by PECVD have comparable or better performance when compared to waveguides fabricated using FHD.

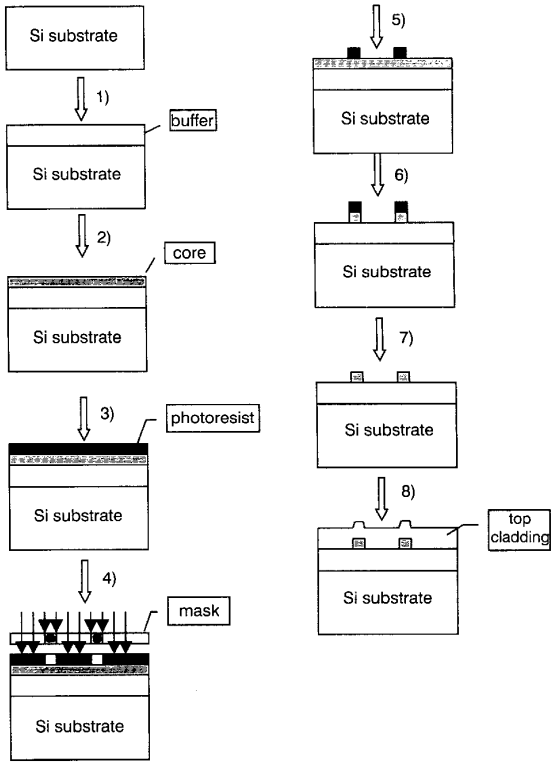

Fig. 1 *Waveguide fabrication flow chart*

Fabrication of waveguides: Waveguide fabrication consists of five main steps: buffer layer growth, core layer deposition, photolithography, core layer etching and top-cladding layer deposition. A flow chart of COM's process is shown in Fig. 1.

In Fig. 1 eight processing steps are indicated and described in the following: 1) wet oxidisation of the silicon wafer forms a thick silica buffer layer; 2) deposition of Ge-doped silica forms the core layer by PECVD; 3) spinning and baking of photoresist on wafer; 4) exposure of photoresist, transferring the waveguide structure from the mask to the photoresist; 5) development of photoresist; 6) etching of the core pattern using RIE; 7) stripping of photoresist; 8) deposition of boron and phosphorus co-doped silica forms top cladding layer by PECVD, with refractive index matched to that of the buffer. This unique processing guarantees good performance of the waveguides.

Because PECVD processing occurs at relatively low temperatures (around 300°C), high temperature annealing is necessary to obtain stable and dense glass. More detailed information about the waveguide fabrication can be found in [6].

For the above processing, the refractive index of the buffer and top-cladding layers are fixed at that of pure glass. To increase the index contrast between the core and the surrounding buffer and top-cladding layers, the index of the core layer must be increased. At the low index contrast region, the refractive index of the core layer increases linearly with GeH4 flow rate. However, this linear relationship does not exist when the GeH4 flow rate is high. Refractive index increases abruptly at some points, and high index contrast becomes difficult to control. When the GeH4 flow rate increases to some point, clusters are formed and the material cannot be used for waveguide fabrication. The index step of 0.02 was chosen as a high index contrast example.

Characterisation of waveguides: The characterisation of waveguides includes measurement of material properties (refractive index and thickness), processing parameters (minimum gap and line reduction)